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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,543	01/13/2004	Jae-goo Lee	5649-951DV	3863

20792 7590 10/07/2004

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EXAMINER	
NHU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,543	LEE, JAE-GOO	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/100,719.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL

DETAILED ACTIONS

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura (6,555,481 B2).

Regarding claim 1, Nakamura, figures 1-24, and related text on col. 1-14, (see figures 9A-9C, 18A-18D, 19A-19D, 20, 22A-22D, col. 8, lines 13-43, col. 10, lines 52-67, col. 11, lines 1-14), disclose an integrated circuit memory device comprising: a semiconductor substrate 1; a plurality of word line (WL) structures 4 b on predetermined portions of the semiconductor substrate; WL contact plugs 7, 8, each of which is deposited between adjacent WL structures; storage node contact plugs 14, SNC in electrical contact with predetermined ones of the WL contact plugs; storage node electrodes 16 on the storage node contact plugs; and plate electrode 18 between the storage node electrodes and between the storage node contact plugs 14, SNC (see figures 9A-9B).

Regarding to claims 2-5, Nakamura, col. 1-14, also teach wherein the plate electrode extends between lower portions of the storage node contact plugs (see figures 22A-22D); a plate insulating layer 13 between the plate electrode 18 and the storage node contact plug 16 that

insulates the plate electrode from the storage node contact plugs; wherein the storage node electrodes are directly on the storage node contact plugs; wherein the WL structures 4, each comprises a gate electrode 4b, a gate insulating layer 4a insulating the gate electrode from the semiconductor substrate, and an insulating material covering a top surface and sides of the gate electrode.

Regarding claim 6, Nakamura, figures 1-24, and related text on col. 1-14, (figures 9A-9D, 18A-18D, 19A-19D, 20, 22A-22D, col. 8, lines 13-43, col. 10, lines 52-67, col. 11, lines 1-14), disclose an integrated circuit memory device comprising: a semiconductor substrate 1; a pair of spaced apart word line (WL) structures 4b on the substrate; an interlayer insulating layer 5, 9 on the WL structures; a bit line (BL) structure 11 on the interlayer insulating layer 9, 5 that is transverse to the WL structures; a first capacitor electrode 16 that extends the substrate between adjacent WL structures through the interlayer insulating layer, and beyond the BL structures; a capacitor dielectric 17 on the first capacitor electrode and directly on the BL structures; and a second capacitor electrode 18 on the capacitor dielectric (see figures 9A-9B). Regarding claims 7, Nakamura, also teach wherein the capacitor dielectric is directly on the interlayer insulating layer.

Regarding claim 8, Nakamura, figures 1-24, and related text on col. 1-14, (see figures 9A-9D, 18A-18D, 19A-19D, 20, 22A-22D, col. 8, lines 13-43, col. 10, lines 52-67, col. 11, lines 1-14), disclose an integrated circuit memory device comprising: a semiconductor substrate 1; a plurality of word line (WL) structures 4b on predetermined portions of the semiconductor substrate; WL contact plugs 7, 8, each of which is deposited between adjacent WL structures; BL structures 11 in electrical contact with a first set of the WL contact plugs; storage node

contact plugs 14, SNC on, and electrically connected to, a second set of the WL contact plugs that is different from the first set of the WL contact plugs; storage node electrodes 16 on the storage node contact plugs; a dielectric layer 17 on the storage node contact plugs and the storage node electrodes; and a plate electrode 18 on the dielectric layer and between the storage node contact plugs 14, SNC and between the storage node electrodes 16. Regarding claims 9-14, Nakamura also teach wherein the plate electrode extends between lower portions of the storage node contact plugs (see figures 22A-22D); a plate insulating layer 13 between the plate electrode 18 and the storage node contact plug 16 that insulates the plate electrode from the storage node contact plugs; wherein the storage node electrodes are directly on the storage node contact plugs; wherein the WL structures 4, each comprises a gate electrode 4b, a gate insulating layer 4a insulating the gate electrode from the semiconductor substrate, and an insulating material covering a top surface and sides of the gate electrode.; the b BL structures each comprises a BL and a dielectric layer on a top surface and sides of the BL.

Response to Arguments

3. Contrary to the applicant's argument about claims 1, 6, 8, in his remarks, Nakamura does not describe/teach storage node contact plugs; a plate electrode on the dielectric layer and between the storage node contact plugs and between the storage node electrodes; a capacitor dielectric on the first capacitor electrode and directly on the bit line structure. In fact, Nakamura clearly teaches storage node contact plugs 14, SNC (see figures 9A-9B); a plate electrode 18 on the dielectric layer 5, 9 and between the storage node contact plugs and between the

storage node electrodes 16, 18; a capacitor dielectric 17 on the first capacitor electrode 16 and directly on the bit line structure 11 (see figures 9B-9C).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kajigaya'365, Aoki'539, Hong'747, Dosaka'628, Ohyu'847, are cited as of interest.

5. A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned(see 710.02 (b)).

6. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571)273-1792.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

David Nhu DN

October 6, 2004